



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,761	08/28/2001	Koji Furusawa	NEC2480-US	3216

466 7590 02/15/2002

YOUNG & THOMPSON  
745 SOUTH 23RD STREET 2ND FLOOR  
ARLINGTON, VA 22202

[REDACTED] EXAMINER

ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<h2 style="margin: 0;">Office Action Summary</h2>	Application No. <b>09/939,761</b>	Applicant(s) <b>Furusawa</b>		
	Examiner <b>Edgardo Ortiz</b>	Art Unit <b>2815</b>		
<i>-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --</i>				
<b>Period for Reply</b>				
<p>A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.</p>				
<ul style="list-style-type: none"> <li>- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.</li> <li>- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.</li> <li>- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.</li> <li>- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).</li> <li>- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).</li> </ul>				
<b>Status</b>				
1) <input checked="" type="checkbox"/> Responsive to communication(s) filed on <u>Aug 28, 2001</u>				
2a) <input type="checkbox"/> This action is FINAL.      2b) <input checked="" type="checkbox"/> This action is non-final.				
3) <input type="checkbox"/> Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11; 453 O.G. 213.				
<b>Disposition of Claims</b>				
4) <input checked="" type="checkbox"/> Claim(s) <u>1-6</u> is/are pending in the application.				
4a) Of the above, claim(s) _____ is/are withdrawn from consideration.				
5) <input type="checkbox"/> Claim(s) _____ is/are allowed.				
6) <input checked="" type="checkbox"/> Claim(s) <u>1-6</u> is/are rejected.				
7) <input type="checkbox"/> Claim(s) _____ is/are objected to.				
8) <input type="checkbox"/> Claims _____ are subject to restriction and/or election requirement.				
<b>Application Papers</b>				
9) <input type="checkbox"/> The specification is objected to by the Examiner.				
10) <input type="checkbox"/> The drawing(s) filed on _____ is/are objected to by the Examiner.				
11) <input type="checkbox"/> The proposed drawing correction filed on _____ is: a) <input type="checkbox"/> approved b) <input type="checkbox"/> disapproved.				
12) <input type="checkbox"/> The oath or declaration is objected to by the Examiner.				
<b>Priority under 35 U.S.C. § 119</b>				
13) <input checked="" type="checkbox"/> Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).				
a) <input checked="" type="checkbox"/> All b) <input type="checkbox"/> Some* c) <input type="checkbox"/> None of: 1. <input checked="" type="checkbox"/> Certified copies of the priority documents have been received. 2. <input type="checkbox"/> Certified copies of the priority documents have been received in Application No. _____ 3. <input type="checkbox"/> Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).				
*See the attached detailed Office action for a list of the certified copies not received.				
14) <input type="checkbox"/> Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).				
<b>Attachment(s)</b>				
15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)				
16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)				
17) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s). <u>3</u>				
18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____				
19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)				
20) <input type="checkbox"/> Other: _____				

## **DETAILED ACTION**

This Office Action is in response to an application filed August 28, 2001.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5 are rejected under 35 U.S.C. § 102 (b) as being anticipated by Takiar et.al. (U.S. Patent No. 5,502,289). With regard to Claim 1, Takiar teaches a semiconductor device with a plurality of semiconductor chips (212, 214) stacked on a substrate (218) wherein the semiconductor device comprises wiring layer (138) disposed so as to be sandwiched between said semiconductor chips and a plurality of bonding pads (234), for connecting a bonding wire, provided on said wiring layer thereto.

With regard to Claim 2, Takiar teaches a connection wiring (230) for connecting among bonding pads provided on a wiring layer (138).

With regard to Claim 3, Takiar teaches a plurality of bonding pads (234) that disposed surrounding a semiconductor chip (216) on an upper surface of the wiring layer (138).

Art Unit: 2815

With regard to Claim 5, Takiar teaches a semiconductor device with a plurality of semiconductor chips (212, 214) stacked on a substrate (218) wherein the semiconductor device comprises wiring layer (138) disposed so as to be sandwiched between said semiconductor chips and a plurality of bonding pads (234), for connecting a bonding wire, provided on said wiring layer thereto and a connection wiring (230) for connecting among said bonding pads provided on a wiring layer (138).

*Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 6 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takiar et.al. (U.S. Patent No. 5,502,289) in view of Tokuda et.al. (U.S. Patent No. 5,870,289). Takiar, as stated supra, essentially discloses the claimed invention but fails to show, a via hole on the wiring layer and connected to a bonding pad of a semiconductor chip. With regard to Claims 4 and 6, Tokuda teaches a chip connection structure having a direct through-hole connection (40) through a wiring layer (20) which connects to a bonding pad (11) of an integrated circuit chip (10).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takiar to include a via hole on

Art Unit: 2815

the wiring layer and connected to a bonding pad of a semiconductor chip, as suggested by Tokuda, in order to achieve high signal transmission and ensure high reliability by the dispersion of stress.

***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

2/7/02



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800